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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,434	07/29/2003	June Lee	4591-338	7848

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,434	LEE, JUNE	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9 and 11-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-14 and 23-26* is/are allowed.

6)☒ Claim(s) *2-5 and 15-22* is/are rejected.

7)☒ Claim(s) *6-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 04/03/2006 has been entered.

2. Claims 12-9,11-26 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 2-9,11-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 2-5,15-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurihara et al. (U.S. Patent No. 6,327,194).

Regarding claim 2, Kurihara et al. disclose a semiconductor memory device (Figure 1) comprising:

a voltage level detector (Figure 1, 106) configured to sense a voltage and configured to generate a power-up signal while the voltage is less than a minimum voltage required to operation device (Column 5, lines 66-67, Column 6, lines 1-11, *generating high voltage for erasing and programming*) ;

a command register (Figure 1, 102) configured to generate a command busy signal;

a read/busy driver controller (Figure 1, State Control) configured to generate a busy enable signal in response to the power-up signal and the command busy signal (Figure 1, 130, Column 5, lines 62-65); and

a read/busy driver configured to drive a read/busy signal in response to the busy enable signal (Figure 1, 130, Column 5, lines 28-29, although figure not shown, but including a driver for input/output ready/busy signal 130).

Regarding claim 3, Kurihara et al. disclose wherein the command register comprises a program command register configured to provide a program busy signal to the read/busy driver controller; and an erase command register configured to provide an erase busy signal to the read/busy driver controller (Column 5, lines 36-51).

Regarding claims 4-5, Kurihara et al. disclose wherein the program busy signal indicates that the memory device is in a program mode or in an erase mode (Column 5, lines 48-50, lines 62-65, programming operation, erase operation, 130 indicates when device is busy undergoing an operation).

Regarding claim 15, Kurihara et al. disclose a semiconductor memory device (Figure 1) comprising:

a voltage level detector (Figure 1, 106) configured to generate a power-up signal (Column 5, lines 66-67, Column 6, lines 1-11, *generating high voltage for erasing and programming*) ;

a command register (Figure 1, 102) configured to generate a command busy signal;

a read/busy driver controller (Figure 1, State Control) configured to generate a busy enable signal in response to the power-up signal and the command busy signal (Figure 1, 130, Column 5, lines 62-65); and

a read/busy driver configured to drive a read/busy signal in response to the busy enable signal (Figure 1, 130, Column 5, lines 28-29, although figure not shown, but including a driver for input/output ready/busy signal 130).

Regarding claim 16, Kurihara et al. disclose wherein the command register comprises a program command register configured to provide a program busy signal to the read/busy driver controller; and an erase command register configured to provide an erase busy signal to the read/busy driver controller (Column 5, lines 36-51).

Regarding claims 17-18, Kurihara et al. disclose wherein the program busy signal indicates that the memory device is in a program mode or in an erase mode (Column 5, lines 48-50, lines 62-65, programming operation, erase operation, 130 indicates when device is busy undergoing an operation).

Regarding 19, Kurihara et al. disclose a method of operating a semiconductor memory device (Figure 1) , the semiconductor memory device including a voltage level detector (Figure 1, 106), a ready/busy driver controller (Figure 1, 102), a ready/busy

driver (Figure 1, 130, *as described above*), and a command register (Figure 1, Command Register), the method comprising:

sensing a voltage with the voltage level detector (Figure 1, voltage Vcc sense with Detector);

generating a power-up signal with the voltage level detector when the voltage is less than a minimum voltage required to operate the semiconductor memory device (Column 5, lines 66-67, Column 6, lines 1-11, *generating high voltage for erasing and programming*); and

generating at least one busy signal with the command register (Figure 1, RY/BY#) , the at least one busy signal indicative of an operational state of the semiconductor memory device (Column 5, lines 62-65); and

generating a busy enable signal with the ready/busy driver controller in response to the power-up signal and the at least one busy signal (Column 5, lines 46-65, RY/BY# response to a signal from 106 and any signal 136-142 and 144 (CE#) inputs to Command register).

Regarding claims 20-21, Kurihara et al. disclose wherein generating a busy signal comprises generating a program busy signal or an erase busy signal (Column 5, lines 48-50, lines 62-65, programming operation, erase operation, 130 indicates when device is busy undergoing an operation).

Regarding claim 22, Kurihara et al. disclose comprising a busy enable signal with ready/busy driver controller, the busy enable signal generated when at least one chosen from the group consisting of power-up signal and the busy signal is at a logic high state

(Column 5, lines 46-65, one of command signals 136-144 high state indicates for an operation is selected and signal from 106 to 102 is high state indicates for a high voltage is used, busy signal 103 is enabled indicates for device is in an operating Column 6, lines 5-10).

Allowable Subject Matter

6. Claims 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-9 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kurihara et al. (U.S. Patent No. 6,327,194), and others, does not teach the claimed invention having a level shifter configured to generate the busy enable signal in response to the first and second control signal as claim 6 disclosed, and an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal as claims 7-9 disclosed.

Claims 11-14, 23-26 are allowed.

Claims 11-14, 23-26 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kurihara et al. (U.S. Patent No. 6,327,194), and others, does not teach the claimed invention having a level shifter configured to generate the busy enable signal in response to the first and second control signal as claims 11, 23

disclosed, and an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal as claims 12-14, 24-26 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

5/31/2006